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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,482	03/12/2004	Akira Takahashi	OKI 414	6303

7590 06/05/2006

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,482	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Applicant's cancellation of claims 6 and 7, and the addition of claims 12 and 13 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The Examiner's rejection of Claims 1 and 3 under 35 U.S.C. 112, first paragraph, is withdrawn in light of the Applicant's amendments dated 4/27/2006.

3. The rejections of Claims 1-11 under 35 U.S.C. 112, second paragraph, are withdrawn in view of the Applicant's amendments dated 4/27/2006. The Applicant has thus made it clear that the term "polysilicon gate" refers to the final gate structure that is formed after the etch of the polysilicon layer is complete.

Claim Objections

4. The Examiner's objections to claims 2, 6 and 9 are withdrawn in light of the Applicant's amendments dated 4/27/2006.

5. Claim 10 is objected to because of the following informalities: The word "or" on line 2 of the claim should be --and--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 and 8-13 are rejected under 35 U.S.C. 103(a) as being anticipated by Gabriel et al. (U.S. Patent # 6541359) in view of Liau et al. (U.S. Patent # 5783850) and further in view of Ker et al. (U.S. Patent # 5637900).

Regarding claim 1, Fig. 5A of Gabriel et al. discloses a semiconductor device comprising:

an N-type polysilicon gate (540, 550) and a P type polysilicon gate (540, 550) (Col. 6, Line 62 – Col. 7, Line 9), both etched simultaneously (Col. 7, Lines 6-9), occupying a first total area; and

Gabriel et al., however, fails to disclose a non-doped polysilicon body disposed adjacent to at least one of the N type polysilicon gate and the P type polysilicon gate, the non-doped polysilicon body occupying a second area larger than the first total area of the N type and P type polysilicon gates.

Fig. 7 of Liau et al. teaches a similar semiconductor device wherein a non-doped polysilicon body (40) disposed adjacent to at least one of the N type polysilicon gate and the P type polysilicon gate (41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the undoped polysilicon body of Liau et al. into the device of

Gabriel et al. The ordinary artisan would have been motivated to modify Gabriel et al. in the above manner for the purpose of combining an ESD protection device with a CMOS circuit device (Liau et al., Col. 2, Lines 35-40).

Gabriel et al. and Liau et al., however, fail to disclose the undoped polysilicon body occupying an area larger than the first total area of the N type and P type polysilicon gates.

Ker et al., however, teaches a similar semiconductor device wherein an ESD transistor has a channel/gate length (2 microns) (Col. 11, Lines 10-13) of greater than twice that of the transistors in the circuit that it is protecting (submicron) (Col. 5, Lines 1-3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the relative gate lengths of the device of Ker et al. into the device of Gabriel et al. and Liau et al. The ordinary artisan would have been motivated to modify Gabriel et al. and Liau et al. in the above manner for the purpose of providing full ESD protection for submicron CMOS technology (Ker et al., Col. 5, Lines 1-3).

Regarding claim 3, Gabriel et al., Liau et al. and Ker et al. disclose a dry etching method (Gabriel et al., Col. 1, Lines 34-38) for a semiconductor device, comprising the following steps of:

simultaneously gate-etching (Gabriel et al., Col. 7, Lines 6-9) an N type polysilicon gate (Gabriel et al., Fig. 5A (540, 550)) and a P type polysilicon gate

(Gabriel et al., Fig. 5A (540, 550)) (Gabriel et al., Col. 6, Line 62 – Col. 7, Line 9); and

setting an etching area (Liau et al., Figs. 4-7 (area of substrate marked 10)) occupied by a non-doped polysilicon body (Liau et al., Fig. 7 (40)), which is adjacent to at least one of the N type polysilicon gate and the P type polysilicon gate (Liau et al., Fig. 7 (41)), larger than a total area of the N type polysilicon gate and the P type polysilicon gate (Ker et al. teaches an ESD transistor having a channel/gate length (2 microns) (Col. 11, Lines 10-13) of greater than twice that of the transistors in the circuit that it is protecting (submicron) (Col. 5, Lines 1-3)).

Regarding claim 8, Gabriel et al., Liau et al. and Ker et al. disclose the semiconductor device according to claim 1, wherein the N type polysilicon gate and the P type polysilicon gate being disposed adjacent to one another (Liau et al., Fig. 7) (the two transistors in the product area 31 are an NMOS and a PMOS transistor).

Regarding claim 9, Gabriel et al., Liau et al. and Ker et al. disclose the dry etching method (Col. 1, Lines 34-38) according to claim 3, wherein the step of simultaneously gate-etching the N type polysilicon gate and the P type polysilicon gate further comprises also etching the non-doped polysilicon body along with the N type polysilicon gate and the P type polysilicon (Liau et al., Col. 2, Line 61 – 1).

Regarding claim 10, Gabriel et al., Liau et al. and Ker et al. disclose the dry etching method (Liau et al., Col. 1, Lines 34-38) according to claim 9, wherein the N type polysilicon gate and the P type polysilicon gate are adjacent one another (Liau et al., Fig. 7) (the two transistors in the product area 31 are an NMOS and a PMOS transistor).

Regarding claim 11, Gabriel et al., Liau et al. and Ker et al. disclose the dry etching method (Col. 1, Lines 34-38) according to claim 3, wherein the N type polysilicon gate and the P type polysilicon gate are disposed adjacent one another (Liau et al., Fig. 7) (the two transistors in the product area 31 are an NMOS and a PMOS transistor).

Regarding claim 12, Gabriel et al., Liau et al. and Ker et al. disclose the semiconductor device of claim 1, wherein the N type polysilicon gate (Liau et al., Fig. 7 (41 (middle transistor))), the P type polysilicon gate (Liau et al., Fig. 7 (41 (far right transistor))), and the non-doped polysilicon body (Liau et al., Fig. 7 (40)) are all etched simultaneously (see rejection, above, of claim 9) from a single polysilicon layer (Liau et al., Figs. 3 and 4 (26))(Liau et al., Col. 4, Lines 10-50).

Regarding claim 13, Gabriel et al., Liau et al. and Ker et al. disclose the dry etching method of claim 3, wherein the N type polysilicon gate (Liau et al., Fig. 7 (41 (middle transistor))), the P type polysilicon gate (Liau et al., Fig. 7 (41 (far right

transistor))), and the non-doped polysilicon body (Liau et al., Fig. 7 (40)) are all etched simultaneously (see rejection, above, of claim 9) from a single polysilicon layer (Liau et al., Figs. 3 and 4 (26))(Liau et al., Col. 4, Lines 10-50).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al. in view of Liau et al., further in view of Ker et al. and further in view of Yoneda (U.S. Patent Publication # 2003/0015763).

Regarding Claim 2, Gabriel et al. discloses N-type and P-type polysilicon gates (Col. 6, Line 62 – Col. 7, Line 9), but fails to specifically disclose the use of boron and phosphorus to dope the gates.

Yoneda teaches a similar semiconductor device wherein P-type and N-type gate electrodes are formed by doping with boron (p-type) and phosphorus (n-type) (Yoneda, Paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the dopants of Yoneda into the device of Gabriel et al., Liau et al. and Ker et al. The ordinary artisan would have been motivated to modify Gabriel et al., Liau et al., and Ker et al. in the above manner for the purpose of knowing what dopants to use to form N-type and P-type gate electrodes (Yoneda, Paragraph 4).

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al. in view of Liau et al., further in view of Ker et al. and further in view of Lee et al. (U.S. Patent # 5665203).

Regarding Claims 4 and 5, Gabriel et al. discloses the dry etching method (Gabriel et al., Col. 1, Lines 34-38) according to claim 3, wherein the etch includes a stage using a mixed gas of HBr and 0_2 (Gabriel et al., Col. 1, Lines 63-65), but fails to disclose the gate etching process being a two-step process, wherein the second step is a stage using a mixed gas of HBr, 0_2 and He.

Lee et al. teaches a similar method wherein the gate etching process is a two-step process which uses a first stage atmosphere of HBr, Cl_2 and He and a second stage atmosphere of HBr, 0_2 and He (Lee et al., Col. 2, lines 39-41).

It would have been obvious to one of ordinary skill in the art to incorporate the method of Lee et al. into the method of Gabriel et al. The ordinary artisan would have been motivated to modify Gabriel et al. in the above manner for the purpose of forming perfectly vertical gate sidewalls (Lee et al. Col. 2, Lines 23-28)

Response to Arguments

9. Applicant's arguments with respect to claims 1-5 and 8-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art discloses similar semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK
05/16/2006

EUGENE LEE
PRIMARY EXAMINER